

Serial No. 10/620,406
Unisys Corporation Docket No. RA-5623

Examiner Lev Iwashko, Group Art Unit 2186
Office Action Response – March 1, 2006

Amendments

In the Claims:

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1 1. (Currently Amended) A memory system, comprising:
2 a programmable storage device to store one or more indicators;
3 a cache;
4 cache tag logic; and
5 a control circuit coupled to the storage device, the cache, and to the cache
6 tag logic, the control circuit to receive data for possible retention in the cache and to
7 determine, based on the state of the one or more indicators, whether to update the
8 cache tag logic to track the data.

1 2. (Currently Amended) The memory system of Claim 1, ~~and further including a~~
2 ~~cache coupled to the cache tag logic to store the data,~~ and wherein the control
3 circuit further includes circuits to determine, based on the one or more indicators,
4 whether to store the data to the cache.

1 3. (Original) The memory system of Claim 2, wherein one of the indicators
2 indicates the cache is not available for use.

1 4. (Original) The memory system of Claim 2, and further including:

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2 at least one requester coupled to the control circuit to request data from, and
3 store data to, the cache;
4 a main memory to provide to the cache requested data that is not stored
5 within the cache; and
6 wherein the control circuit includes a circuit that may replace the data in the
7 cache based on the state of the indicators.

1 5. (Original) The memory system of Claim 4, wherein the main memory provides
2 data to the cache in response to a request that is any one of multiple request types,
3 wherein at least one of the indicators identifies one or more of the request types, and
4 wherein the control circuit prevents the replacement of the data in the cache if the
5 data was provided in response to any of the identified request types.

1 6. (Original) The memory system of Claim 4, wherein the one or more request
2 types includes a request type indicating the data will be modified by a requester.

1 7. (Original) The memory system of Claim 4, wherein at least one of the
2 indicators identifies one or more of the at least one requester, and wherein the
3 control circuit replaces the data in the cache if the data was returned from the main
4 memory in response to a request issued by any of the identified requesters.

1 8. (Original) The memory system of Claim 4, wherein the main memory
2 provides data to the cache with a response that is any one of multiple response

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3 types, wherein at least one of the indicators identifies one or more of the response
4 types, and wherein the control circuit replaces the data in the cache if the data is
5 returned from the main memory with any of the identified response types

1 9. (Original) The memory system of Claim 2, and further including at least one
2 requester coupled to the control circuit to return data to the cache tag logic, and
3 wherein the control circuit determines whether to store the returned data to the
4 cache based on the state of at least one of the indicators.

1 10. (Original) The memory system of Claim 9, wherein the at least one requester
2 returns data to the cache tag logic during an operation that is any one of multiple
3 operation types, wherein the indicators include an indicator to identify one or more of
4 the operation types, and wherein the control circuit stores the returned data to the
5 cache if the returned data is returned during any of the identified operation types

1 11. (Original) The memory system of Claim 10, wherein the control circuit is
2 further adapted to store the returned data to the cache based, at least in part, on
3 whether a cache hit occurred.

1 12. (Original) The memory system of Claim 9, and further including a main
2 memory coupled to the control circuit, and wherein the control circuit is adapted to
3 forward the returned data to the main memory based, at least in part, on the state of
4 at least one of the indicators.

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1 13. (Original) The memory system of Claim 12, wherein memory coherency
2 actions may be incomplete for the returned data or for associated data retained by
3 the at least one requester or the cache, and further including a request tracking
4 circuit coupled to the control circuit to prevent the returned data from being
5 forwarded to the main memory until all of the memory coherency actions have been
6 completed for the returned data or for the associated data.

1 14. (Original) The memory system of Claim 1, wherein the programmable
2 storage device includes circuits to store microcode, and wherein the control circuit is
3 controlled by the microcode..

1 15. (Original) The method of Claim 1, and further including mode switch logic
2 coupled to the programmable storage device to automatically re-program at least
3 one of the indicators in response to monitored conditions occurring within the
4 memory system.

1 16. (Currently Amended) A method of controlling a memory system having cache
2 tags to record which data is stored within one or more associated caches, and
3 further having one or more programmable control indicators, comprising:
4 a.) obtaining data; and
5 b.) determining whether to update the cache tags to record the data based on
6 the state of one or more of the control indicators.

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1 17. (Currently Amended) The method of Claim 16, ~~wherein the memory system~~
2 ~~includes a cache~~, and further including determining whether to store the data in a
3 predetermined one of the associated caches ~~cache~~ based on the state of one or
4 more of the control indicators.

1 18. (Original) The method of Claim 17, wherein the memory system includes a
2 main memory coupled to the cache tags, and wherein the obtaining step includes:
3 providing a request for the data to the main memory; and
4 receiving the data from the main memory.

1 19. (Original) The method of Claim 18, wherein the request is any one of multiple
2 types, wherein one of the control indicators identifies one or more of the multiple
3 request types, and wherein at least one of the determining steps is performed
4 based, at least in part, upon whether the request is any of the identified response
5 types.

1 20. (Original) The method of Claim 18, wherein the data is provided from the
2 main memory with a response type that is any one of multiple response types,
3 wherein one of the control indicators identifies one or more of the multiple response
4 types, and wherein at least one of the determining steps is performed based, at least
5 in part, upon whether the request is any of the identified response types.

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1 21. (Original) The method of Claim 18, wherein the memory system is coupled to
2 at least one requester, wherein one of the control indicators identifies one or more of
3 the at least one requester, and wherein at least one of the determining steps is
4 performed based, at least in part, upon whether the request was initiated by any of
5 the identified requesters.

1 22. (Original) The method of Claim 17, wherein the memory system is coupled to
2 at least one requester, and wherein step a.) includes obtaining the data from any
3 one of the at least one requester.

1 23. (Original) The method of Claim 22, wherein the data is obtained during an
2 operation that is any of multiple operation types, wherein one of the control
3 indicators identifies one or more of the operation types, and wherein at least one of
4 the determining steps is based, at least in part, on whether the data is obtained
5 during any of the identified operation types.

1 24. (Original) The method of Claim 23, wherein at least one of the determining
2 steps is based, at least in part, on whether a cache hit occurs.

1 25. (Currently Amended) The method of Claim 22, wherein the memory system
2 includes a main memory, and further including providing the data to the main
3 memory instead of storing the data into the predetermined one of the associated
4 caches ~~cache~~.

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1 26. (Original) The method of Claim 25, wherein the data is associated with
2 incomplete memory coherency actions, and further including preventing the data
3 from being provided to the main memory until all incomplete memory coherency
4 actions have been completed.

1 27. (Original) The method of Claim 16, and further comprising:
2 c.) monitoring conditions within the memory system; and
3 d.) automatically re-programming at least one of the control indicators based
4 on one or more of the monitored conditions.

1 28. (Currently Amended) A memory system, comprising:
2 main memory means for storing data;
3 cache means for storing a subset of the data; and
4 programmable storage means for storing control indicators to determine how
5 ~~select~~ the subset of the data is to be selected.

1 29. (Original) The memory system of Claim 28, wherein requests are issued to
2 the main memory to retrieve data from the main memory, and wherein the
3 programmable storage means includes means for selecting the subset of the data
4 based, at least in part, on a type of request that was issued to retrieve the subset of
5 the data from the main memory.

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1 30. (Currently Amended) The memory system of Claim 28, and further including
2 one or more requester means for causing data to be retrieved from the main
3 memory, and wherein the programmable storage means includes means for
4 selecting the subset of the data based, at least in part, on the ~~identify~~ identity of one
5 or more of the requester means that caused data to be retrieved from the main
6 memory.

1 31. (Original) The memory system of Claim 28, wherein the main memory means
2 includes means for returning a response type to the cache means with data, and
3 wherein the programmable storage means includes means for selecting the subset
4 of the data based, at least in part, on the response type.

1 32. (Original) The memory system of Claim 28, and further including requester
2 means for returning data to the cache means, and wherein the programmable
3 storage means includes means for selecting whether data returned by the requester
4 means will be stored to the cache means.

1 33. (Original) The memory system of Claim 32, wherein the requester means
2 includes means for returning data during any of multiple types of operations, and
3 wherein the programmable storage means includes means for selecting whether
4 returned data will be stored to the cache means based, at least in part, on the type
5 of operation that resulted in return of the data.

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1 34. (Original) The memory system of Claim 32, wherein the programmable
2 storage means includes means for selecting whether data returned by the requester
3 means will be stored to the cache means based, at least in part, on whether a cache
4 miss occurred to the cache means.

1 35. (Original) The memory system of Claim 28, and further including mode
2 switch means for modifying the state of one or more of the control indicators based
3 on monitored conditions occurring within the memory system.

1 36. (Original) The memory system of Claim 28, and wherein the cache means
2 includes cache tag means for tracking data that may be stored to the cache means,
3 and wherein the programmable storage means includes means for determining
4 whether to update the cache tag means to track data.

1 37. (Original) The memory system of Claim 36, wherein the programmable
2 storage means includes means for enabling the tracking by the cache tag means of
3 predetermined data that is not included in the subset of the data stored within the
4 cache means.

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